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RESEARCH ARTICLE

A Novel Single-Source 13-Level Switched-Capacitor Inverter With Triple Voltage Gain

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ABSTRACT In recent years, the growing demand for efficient voltage boosting solutions has been driven by advancements in renewable energy systems, electric vehicles (EVs), and photovoltaic (PV) arrays. However, conventional magnetic-based inverters remain bulky and inefficient for compact, high-performance applications, limiting their use in emerging technologies. To address this, the objective of this study is to develop a compact, single-source switched-capacitor multilevel inverter (SC-MLI) topology that achieves high voltage gain with minimal component count. The proposed 13-level SC-MLI employs a novel switched-capacitor structure and is evaluated under Natural Level Control (NLC) and Sinusoidal PWM (SPWM) schemes. Theoretical analysis, MATLAB/Simulink simulations, and experimental validation on a 100–1000 W prototype are carried out, along with thermal modeling in PLECS. The results show that the topology achieves a voltage gain of 3, maintains capacitor self-balancing without auxiliary circuits, and reaches a peak efficiency of 97.2% (simulation) and 95.3% (experiment). Moreover, it meets harmonic standards, reduces total harmonic distortion (THD), and outperforms recent single-source designs in terms of accuracy, cost, and control simplicity. This makes the proposed topology highly suitable for grid-connected PV systems, electric vehicle chargers, and compact renewable energy interfaces, with theoretical scalability toward medium- and high-power applications.

INDEX TERMS Multilevel inverter, self-voltage balancing, switched capacitor (SC), triple voltage gain.

I. INTRODUCTION

In recent years, the increasing use of renewable energy sources [1] and the increasing integration of high power density batteries into systems have significantly increased the demand for multilevel inverters (MLI) in the field of power electronics [2]. Many applications today require high efficiency, high power density, low harmonic distortion and good quality input voltage. Thanks to their structural advantages, MLIs offer superior power quality with low switching voltage stress, high output voltage level and low harmonic distortion in DC-AC conversion. Thanks to these advantages, MLIs have become a fundamental power converter element in many industrial fields such as electric vehicles (EV), high frequency AC power distribution (HFACPD), renewable energy systems, microgrids and charging infrastructures [3]. However, conventional MLI topologies such as Cascaded H-Bridge (CHB), Neutral Point Clamped (NPC) and Flying Capacitor (FC) structures require a large number of semiconductor elements. In addition, multiple isolated DC voltage sources are needed in the CHB structure, while FC inverters require additional balancing circuits to stabilize the capacitor voltages. In order to achieve higher output levels, the system complexity increases and more advanced control algorithms are needed [4], [5].

The switched capacitor (SC) approach offers significant advantages such as compact structure, low weight and high power density due to its inductorless DC-DC conversion

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capability. With these features, it provides an effective solution to the problems commonly encountered in MLI circuits such as the need for multiple input voltages and self-voltage stabilization [6], [7]. The voltage boost function of SC-MLIs can be realized by switching capacitors in series-parallel with the source without the need for large and heavy transformers. On the other hand, there are some MLI topologies based on high frequency magnetic transformers for voltage amplification [8].

SC-MLI structures can provide voltage boost without the use of conventional heavy inductors, while the self-voltage stabilization of capacitors eliminates the need for complex stabilization circuits. Since these topologies include switching loops that passively stabilize the capacitor voltages, the system is both low volume and low cost, and the control structure becomes extremely simplified [9].

SC-MLI topologies in the literature are generally classified according to three main categories: the number of DC sources used at the input side (single or multiple), the voltage boost ratio achieved and the output voltage levels. High power density can be achieved by optimizing these parameters according to the specific needs of the applications [10]. Some topologies require an H-bridge at the output, while others are capable of generating bipolar output levels directly. Configurations using multiple capacitors usually have more than one voltage boost capability [11]. However, since SCs operate with continuous charge and discharge cycles, it may not be possible to generate a constant DC voltage at the output. This leads to voltage fluctuations that cause low-order harmonic components in the output waveform [12]. 13-level SC-MLI structures are prominent in many studies [13]. To achieve high output levels, a large number of power components and multiple DC sources are required. Although various SC-based topologies with multiple DC sources have been developed [14], there is an increasing requirement of single DC source solutions for applications such as electric vehicles (EVs) and renewable energy systems. In this context, research on single-source SC-MLI structures has been accelerated [15].

In order to fully utilize the advantages of single-source systems, it is crucial to reduce the total number of components in the circuit. In this regard, many researchers have tried to minimize the number of switches and passive elements to reduce the circuit complexity. A notable contribution in this context is presented in [16], where an innovative 17-level MLI topology is proposed using only 10 power switches, a soft-charging cell (SCC), and a high-frequency link (HFL) unit to achieve high voltage gain and reduced transformer size. With a cost function (CF) of 1.60 and an efficiency of 96.92%, the topology demonstrates promising performance in renewable energy and EV applications. In [17] and [18], both structures provide 6-fold voltage amplification with a single DC source and produce 13-level output. In [17], four switches are saved by using an additional capacitor. There have also been many studies on 9-level SC-MLI topologies, which are considered intermediate in the literatures [14] and [19]. However, in these designs, a significant reduction in the number of components is usually not achieved. For example, in [14], although the number of switches was reduced to 9, 4 capacitors and 4 separate diodes were still used. Similarly, in [20], a total of 17 power switches are required to achieve the same level. In general, as the output voltage level decreases, the total number of components required to achieve this level increases proportionally, which severely increases the voltage stress on the switches [21].

In this paper, a new SC-MLI topology is proposed that operates with a smaller number of power components compared to most of the existing structures in the literature. The proposed structure uses only 11 switches, 3 capacitors and 3 discrete diodes to produce a 13-level output voltage. In terms of the total number of power components per level, the proposed structure is one of the least component-intensive alternatives. This result can be explained by the cost function (CF), which is widely used in the comparison of MLI circuits. CF is a fundamental criterion to evaluate the economic efficiency of the system.

The presented 13-level SC-MLI structure makes a significant contribution to the literature with a low CF value of 2.36 and a high efficiency ratio of 92.7%. Its self-voltage stabilization capability eliminates the need for additional stabilization circuits, which simplifies the control algorithm. The proposed SCMLI topology has been theoretically validated and experimentally tested on a low-power prototype. Although suitable for medium-voltage and high-power applications in theory, practical implementation would require high-voltage-rated switches and advanced insulation and thermal management strategies. The ability to generate 13 levels using a single DC source makes it ideal for high-voltage applications. The proposed topology is simulated using both fundamental frequency modulation and high frequency pulse width modulation techniques. Experimental studies on the prototype circuit are compared with the simulation results and their accuracy is verified. The results are compared with the existing literature and the advantages of the proposed scheme are discussed in detail.

II. PROPOSED SC-MLI TOPOLOGY

The proposed switched capacitor multilevel inverter (SC-MLI) topology is shown in detail in Fig. 1. The main circuit structure consists of a single DC power supply, ten power switches (H_1-H_4, S_1-S_5 and S_1'), three capacitors (C_1, C_2 and C_3) and three discrete diodes (D_1, D_2 and D_3). This structure is capable of producing a 13-level output voltage using only one DC input source. A threefold amplification of the output voltage is achieved by switched capacitors integrated into the system.

The system allows energy transfer from the DC source to both the load and the capacitors via different switching combinations. Capacitor C_1 is directly charged by the source voltage (V_{DC}), whereas capacitors C_2 and C_3 share the

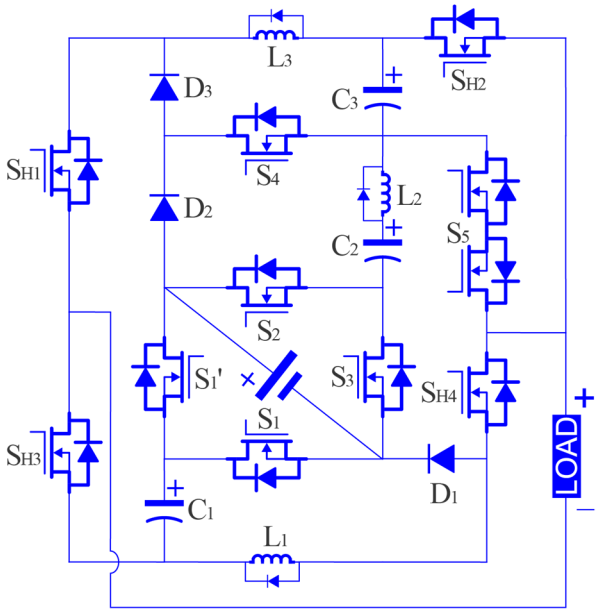


FIGURE 1. Proposed topology of the SC-MLI.

TABLE 1. Switching pattern and capacitor effects.

[$S_{H4}S_{H3}S_{H2}S_{H1}$ - $S_1S_2S_3S_4S_5$]	V_L	[$C_1C_2C_3$]	[$D_1D_2D_3$]
States of the Switches			
[1001-11000]	+6	▼▼▼	[000]
[1001-10010]	+5	▼ – ▼	[010]
[1001-10100]	+4	▼▲▲	[011]
[1001-00010]	+3	▲ – ▼	[110]
[1001-00100]	+2	▲▲▲	[111]
[0001-00101]	+1	▲▲▲	[111]
[0011-00100]	+0	▲▲▲	[111]
[0100-00101]	-1	▲▲▲	[111]
[0110-00100]	-2	▲▲▲	[111]
[0100-01001]	-3	▲▼ –	[100]
[0110-10100]	-4	▼▲▲	[011]
[0100-11001]	-5	▼▼ –	[000]
[0110-11000]	-6	▼▼▼	[000]

▲ Charging ▼ Discharging – No Effect

voltage equally. As a result, the terminal voltages of the capacitors are $V_{C1} = V_{DC}$, $V_{C2} = 0.5V_{DC}$, and $V_{C3} = 0.5V_{DC}$, respectively. This configuration effectively amplifies the output voltage of the main circuit by three times the source voltage. Here, VDC represents the magnitude of the constant DC source voltage applied at the input of the circuit.

Fig. 2 shows the load and capacitor current loops for positive, negative and zero output voltage levels. The load current cycles (capacitor discharging currents) at different switching states are shown with red color, while the capacitor charging cycles are shown with green color. Fig. 2 also shows that the proposed SC-MLI structure generates 13 different voltage levels at the output by means of only one DC source and series connection of capacitor voltages in various switching states.

The switching states and capacitor charge/discharge states are presented in Table 1. Since the S_1 and S_1' switches work inversely to each other, it is sufficient to indicate only the state of the S_1 switch in the table.

Since the input voltage source has a magnitude of V_{DC}, the capacitors are charged as follows: $V_{C1} = V_{DC}$, $V_{C2} = 0.5V_{DC}$, and $V_{C3} = 0.5V_{DC}$. The operating modes corresponding to each voltage level are illustrated in Fig. 2. Single-polarity voltage levels are described individually due to their derivation from distinct capacitor combinations, whereas symmetric voltage levels are generated from the same configurations and are therefore not detailed separately.

A. VOLTAGE BALANCING AND CHARGING OF CAPACITORS

One of the major challenges in SC-MLI topologies is achieving voltage balance across the capacitors. Many of these configurations require complex control algorithms to actively regulate and equalize capacitor voltages during operation. In contrast, the SC-MLI topology proposed in this study inherently eliminates the need for such control complexity due to its self-balancing voltage mechanism. The natural charging and discharging behavior of the capacitors ensures stable operation without auxiliary balancing circuits. Fig. 3 illustrates the capacitor charging/discharging states, the corresponding output voltage waveform, and the associated switching pulses for the proposed topology.

As depicted in Fig. 2, capacitor C_1 is connected in parallel with the DC voltage source via switch S_1', and the path for the charging current is indicated in green. Fig. 3 shows the time intervals (t_0-t_4) when the S_1' switch is in conduction at the output voltage levels of 0, ±1 V_{DC}, ±2 V_{DC} and ±3 V_{DC}, indicating that capacitor C_1 is in charging mode. C_1 discharges by feeding the load at ±4 V_{DC}, ±5 V_{DC} and ±6 V_{DC} output levels. This period defines the maximum discharge time (MDT) for C_1 and should be considered when determining the capacitor value. The MDT for C_1 is expressed as $MDT_{C1} = T/2 - 2t_4$.

The configuration of capacitors C_2 and C_3 is also shown in Fig. 2. These capacitors are charged by connecting them in parallel to a DC voltage source at ±1 V_{DC}, ±2 V_{DC} and ±4 V_{DC} output levels. In these modes, both capacitors are fully charged to half the amplitude of the DC source ($V_{C2} = V_{DC}$, $V_{C3} = V_{DC}$). The MDT occurs in the positive half cycle for C_3 and in the negative half cycle for C_2. However, since they cover ±5 V_{DC} and ±6 V_{DC} levels, the MDT time of both capacitors is equal and is expressed as $MDT_{C3} = MDT_{C2} = T/2 - 2t_5$.

Capacitor C_2 is discharged at $+3$ V_{DC} and $+5$ V_{DC} output levels, while C_3 is discharged at -3 V_{DC} and -5 V_{DC}. Since the other corresponding capacitor is disabled at these levels, it has no effect.

Moreover, as seen in Fig. 2, during the $+1$V output level, both C_2 and C_3 are charged by the DC source, while C_3

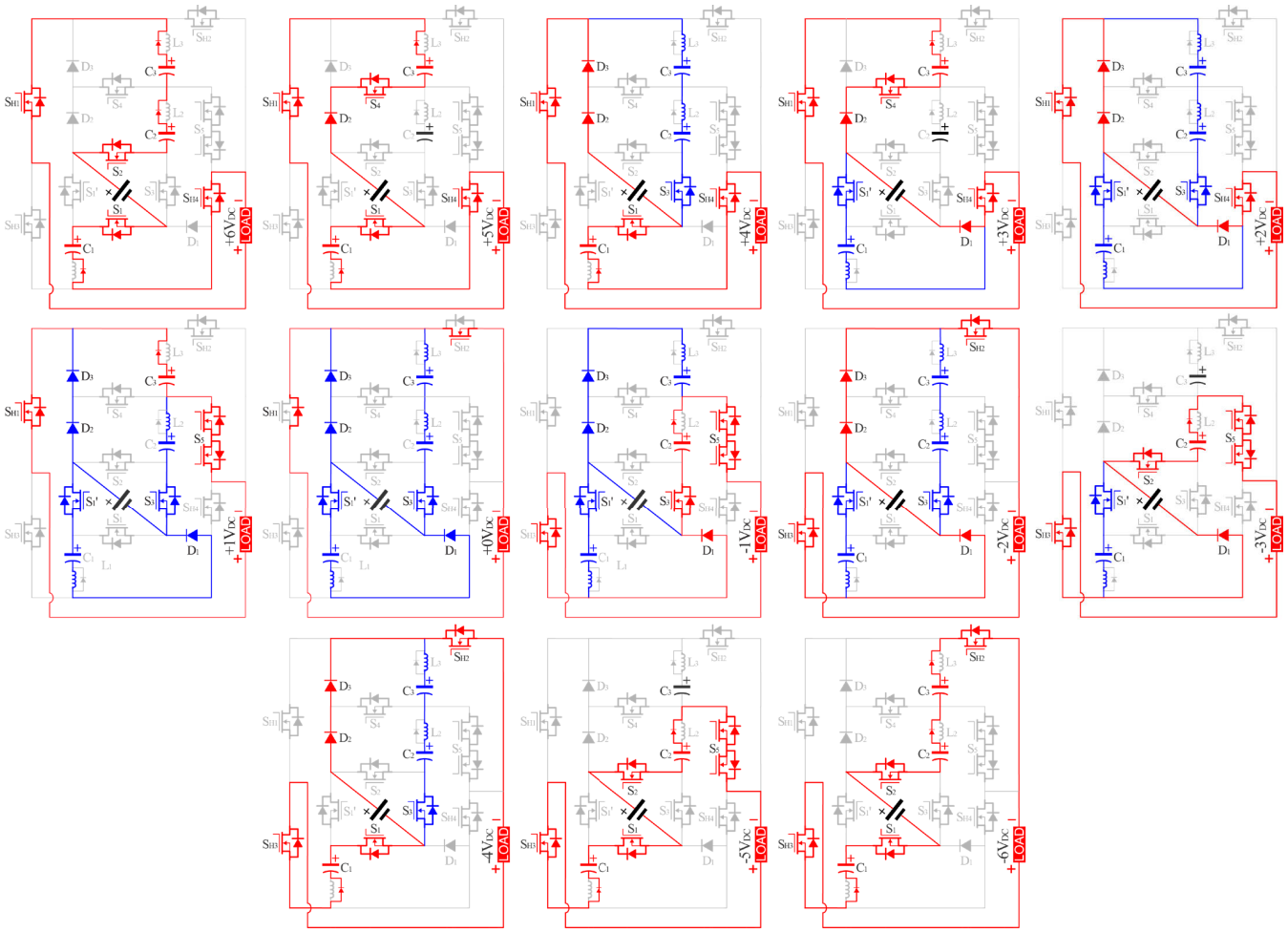


FIGURE 2. Operating modes for all output voltage levels.

also conducts load current. Despite this, C_3's voltage remains stable due to simultaneous charging from the source. This is confirmed by the capacitor voltage waveforms in Fig. 3, where no significant voltage drop is observed on C_3.

B. DESIGN OF CAPACITORS AND INDUCTORS

In SC-MLI topologies, capacitors are charged and discharged intermittently during each switching cycle, thereby maintaining the desired output voltage levels. The output waveform is affected by both the DC input source and the voltage across each individual capacitor. During discharge, the load current causes voltage fluctuations in the capacitors; this fluctuation is typically limited to 5-10% of the nominal voltage to ensure stable operation.

To keep this fluctuation within acceptable limits, capacitor sizing is determined based on MDT and load current. The voltage fluctuation across capacitor i is expressed as follows:

$$\Delta v_{Ci} = \frac{\Delta Q_{Ci}}{C_i} = \frac{1}{C_i}\int_{t_a}^{t_b} i_L dt \tag{1}$$

where i_L is the load current and $t_a - t_b$ is the discharge interval. In the topology, the MDTs for capacitors are:

$MDT_{C1} = t_4 - (T/2 - t_4)$ and $MDT_{C2} = MDT_{C3} = t_5 - (T/2 - t_5)$

Using this, the capacitance values are selected to limit voltage ripple to under 10% of the input voltage ($V_{in} = 60V$) for a load of $R = 150\Omega$ in series with 50 mH inductance. Accordingly: $C_1 = 2200\ \mu F$ and $C_2 = C_3 = 1200\mu F$. These values ensure that the capacitor voltages remain within the acceptable fluctuation limits across all operating conditions.

The inductors used in the soft-charging circuit are designed to suppress high peak currents during the capacitor charging period, which helps reduce ripple losses and enhances overall efficiency. To effectively limit the di/dt stress on switching components and to ensure soft charging, an appropriate inductance value must be selected [22].

According to the literature, the inductor value is typically chosen such that the ripple current (ΔI_L) falls within 20%–40% of the input current. A lower ΔI_L improves filtering but increases the inductor size and cost. A common design practice is to set ΔI_L at approximately 30% of the average input current for a balanced trade-off between performance and size.

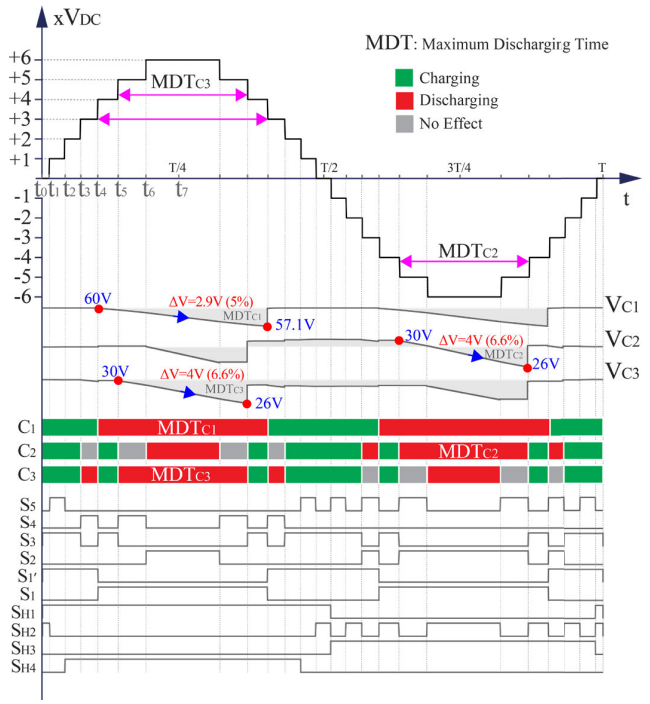


FIGURE 3. Output voltage waveform of the proposed SC-MLI, showing capacitor charge/discharge states and corresponding switch pulses.

The minimum required inductance L_C is calculated based on the minimum input voltage, desired current ripple, and switching frequency, using the following equation:

$$L_C = \frac{V_{in,\min}}{f_{sw} \cdot \Delta I_L \cdot \frac{V_{in}}{V_C}} \tag{2}$$

where $V_{in,min}$ is the minimum input voltage, f_{sw} is the switching frequency, ΔI_L is the allowed ripple current (typically 20%–40% of input current), and V_C is the voltage across the capacitor. The inductors in the proposed circuit were selected as 80μH based on (2) to ensure reliable soft-charging operation.

III. POWER LOSS ANALYSIS

In power electronic circuits, the total power loss (P_{LOSS}) arises from the voltage drops across the components present in the current path. These losses primarily include the conduction losses (P_{Con}) due to the on-state voltage drops of switches and diodes, the switching losses (P_{SW}) during transitions of the switching devices, and the ripple losses (P_{ripple}) caused by voltage fluctuations across the capacitors. Accordingly, the total power loss of the system can be expressed as given in (3)

$$P_{Loss} = P_{Con} + P_{Sw} + P_{Ripple} \tag{3}$$

A. CALCULATION OF CONDUCTION LOSS, P_{CON}

As load current flows through the internal resistance (R_{ON}) of power switches, the resistance of diodes (R_D) and the resistance of capacitors (R_C) in the open position in the circuit, it causes P_{Con}. These losses are due to the non-ideal characteristics of the components in the conduction state and the series resistance of the capacitors. Conduction loss for each output level varies depending on the power components in the current path specific to that level. Therefore, the equivalent conduction circuits for each output level of the SC-MLI topology are presented in Table 2. In these circuits, the charge/discharge currents of the capacitors and the load current cause instantaneous power variations. Since the output waveform is stepped as shown in Fig. 3, the conduction losses should be calculated based on the average power considering the time intervals of each level. According to Table 2, the equivalent circuits for positive and negative half waves are the same at $\pm 2V_{DC}$, $\pm 4V_{DC}$ and $\pm 6V_{DC}$ levels. At other levels, the positive and negative directional circuit structures differ. Also, in the waveform in Fig. 3, all levels occur with equal times in the positive and negative half-wave. These time intervals in the positive half-wave are $\Delta t_{\pm i} = t_{i+1}$-$t_i$, $\Delta t_0 = t_1$, $\Delta t_{\pm 6} = T/2$-t_6.

Here, Δt_{-i} represents the duration of the negative i_{th} voltage level, Δt_{+i} the duration of the positive i_{th} voltage level, T denotes the total duration of a switching period.

Using the equivalent circuits in Table 2, the average power calculations for the abovementioned periods are expressed as follows:

$$P_{Con} = \sum_{j=-n}^{n} P_{Con_j} \tag{4}$$

$$P_{Con_j} = \frac{1}{T} \int_T p_{Con_j} dt \tag{5}$$

$$P_{Con_j} = \frac{1}{T} \sum_T \Delta t_j p_{Con_j} \tag{6}$$

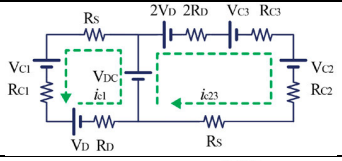
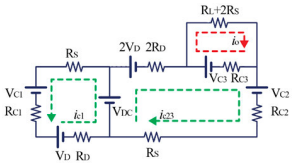
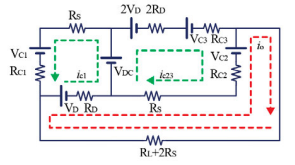
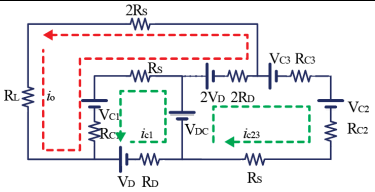
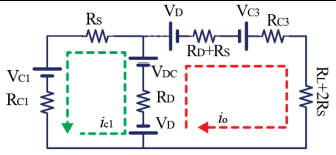
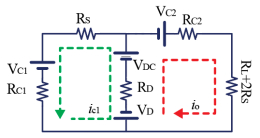
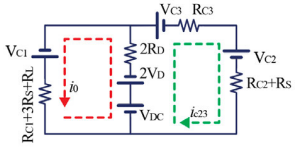
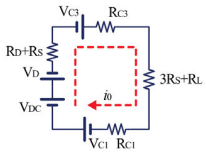
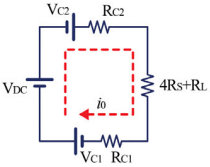
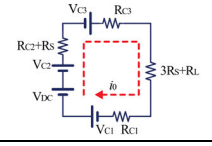
If the internal resistance of the power components and the capacitor voltages remain constant, the instantaneous power at each output level can be considered constant.

The integral expression given in (5) can be converted into a discrete summation, as demonstrated in (6). In this formulation, n indicates the count of positive output voltage levels generated by the inverter. $P_{Con,j}$ stands for the mean conduction power at the j-th level, whereas $p_{Con,j}$ refers to the real-time conduction power for that level. The aggregate time duration for all levels during one complete switching period is represented by $\sum(\Delta tj)$, where Δtj signifies the time span allocated to the j-th level.

$$p_{Con_j} = i_k^2 R_{eq_i} \tag{7}$$

For the i-th output level, $R_{eq,i}$ describes the overall equivalent resistance in the circuit, and ik indicates the current flowing through the k-th branch. By applying Kirchhoff's Current Law to the equivalent circuit models provided in Table 2, the branch currents can be systematically determined. This enables the theoretical computation of the instantaneous conduction loss $p_{con,j}$ at each level. As an example, when operating at the +1 level, the equivalent circuit consists of three distinct loops. The branch currents

TABLE 2. Equivalent circuits and conduction loss equations for all output voltage levels.

Levels	Equivalent Circuit	Current Equations	Power Equations
0		$i_{C1}=\frac{V_{DC}-V_{C1}-V_D}{R_{C1}+R_D+R_S};\quad i_0=0$ $i_{C2}=i_{C3}=\frac{V_{DC}-2V_D-V_{C2}-V_{C3}}{R_{C2}+R_{C3}+2R_D+R_S}$	$p_{c0}=i_{C1}^2\left(R_{C1}+R_D+Rs\right)$ $+i_{C2}^2\left(R_{C2}+R_{C3}+2R_D+Rs\right);$ $P_{c0}=\frac{4t_1}{T}p_{c0}$
+1 V_{DC}		$i_0=\frac{V_{C3}}{R_{C3}+2R_S+R_L};$ $i_{C1}=\frac{V_{DC}-V_{C1}-V_D}{R_{C1}+R_D+R_S};$ $i_{C2}=i_{C3}=\frac{V_{DC}-2V_D-V_{C2}-V_{C3}}{R_{C2}+R_{C3}+2R_D+R_S}$	$p_{c1}=i_0^2\left(R_{C3}+R_L+2Rs\right)$ $+i_{C1}^2\left(R_{C1}+R_D+Rs\right)$ $+i_{C2}^2\left(R_{C2}+R_{C3}+2R_D+Rs\right);$ $P_{c1}=\frac{2(t_2-t_1)}{T}p_{c1}$
-1 V_{DC}		$i_0=\frac{V_{C2}-V_D}{R_{C2}+R_D+3R_S+R_L};$ $i_{C1}=\frac{V_{DC}-V_{C1}-V_D}{R_{C1}+R_D+R_S};$ $i_{C2}=i_{C3}=\frac{V_{DC}-2V_D-V_{C2}-V_{C3}}{R_{C2}+R_{C3}+2R_D+R_S}$	$p_{c-1}=i_0^2\left(R_{C2}+R_D+R_L+3Rs\right)$ $+i_{C1}^2\left(R_{C1}+R_D+Rs\right)$ $+i_{C2}^2\left(R_{C2}+R_{C3}+2R_D+Rs\right);$ $P_{c-1}=\frac{2(t_2-t_1)}{T}p_{c-1}$
±2 V_{DC}		$i_0=\frac{V_{C1}-2V_D}{R_{C1}+2R_D+3R_S+R_L};$ $i_{C1}=\frac{V_{DC}-V_{C1}-V_D}{R_{C1}+R_D+R_S};$ $i_{C2}=i_{C3}=\frac{V_{DC}-2V_D-V_{C2}-V_{C3}}{R_{C2}+R_{C3}+2R_D+R_S}$	$p_{c2}=i_0^2\left(R_{C1}+2R_D+3Rs+R_L\right)$ $+i_{C1}^2\left(R_{C1}+R_D+Rs\right)$ $+i_{C2}^2\left(R_{C2}+R_{C3}+2R_D+Rs\right);$ $P_{c2}=\frac{4(t_3-t_2)}{T}p_{c2}$
+3 V_{DC}		$i_0=\frac{V_{DC}+V_{C3}-2V_D}{R_{C3}+2R_D+3R_S+R_L};$ $i_{C1}=\frac{V_{DC}-V_{C1}-V_D}{R_{C1}+R_D+R_S};$ $i_{C2}=0;\quad i_{C3}=i_0$	$p_{c3}=i_0^2\left(R_{C3}+2R_D+3Rs+R_L\right)$ $+i_{C1}^2\left(R_{C1}+R_D+Rs\right);$ $P_{c3}=\frac{2(t_4-t_3)}{T}p_{c3}$
-3 V_{DC}		$i_0=\frac{V_{DC}+V_{C2}-V_D}{R_{C2}+R_D+2R_S+R_L};$ $i_{C1}=\frac{V_{DC}-V_{C1}-V_D}{R_{C1}+R_D+R_S};$ $i_{C2}=i_0;\quad i_{C3}=0$	$p_{c-3}=i_0^2\left(R_{C2}+R_D+2Rs+R_L\right)$ $+i_{C1}^2\left(R_{C1}+R_D+Rs\right);$ $P_{c-3}=\frac{2(t_4-t_3)}{T}p_{c-3}$
±4 V_{DC}		$i_0=\frac{V_{DC}+V_{C1}-2V_D}{R_{C1}+2R_D+3R_S+R_L};$ $i_{C2}=i_{C3}=\frac{V_{DC}-2V_D-V_{C2}-V_{C3}}{R_{C2}+R_{C3}+2R_D+R_S};$ $i_{C1}=0;$	$p_{c4}=i_0^2\left(R_{C1}+2R_D+3Rs+R_L\right)$ $+i_{C2}^2\left(R_{C2}+R_{C3}+2R_D+Rs\right);$ $P_{c4}=\frac{4(t_5-t_4)}{T}p_{c4}$
+5 V_{DC}		$i_0=\frac{V_{DC}+V_{C1}+V_{C3}-V_D}{R_{C1}+R_{C3}+R_D+4R_S+R_L};$ $i_{C1}=i_{C3}=i_0;$ $i_{C2}=0;$	$p_{c5}=i_0^2\left(R_{C1}+R_{C3}+R_D+4Rs+R_L\right);$ $P_{c5}=\frac{2(t_6-t_5)}{T}p_{c5}$
-5 V_{DC}		$i_0=\frac{V_{DC}+V_{C1}+V_{C2}}{R_{C1}+R_{C2}+4R_S+R_L};$ $i_{C1}=i_{C2}=i_0;$ $i_{C3}=0;$	$p_{c-5}=i_0^2\left(R_{C1}+R_{C2}+4Rs+R_L\right);$ $P_{c-5}=\frac{2(t_6-t_5)}{T}p_{c-5}$
±6 V_{DC}		$i_0=\frac{V_{DC}+V_{C1}+V_{C2}+V_{C3}}{R_{C1}+R_{C2}+R_{C3}+4R_S+R_L};$ $i_{C1}=i_{C2}=i_{C3}=i_0;$	$p_{c6}=i_0^2\left(R_{C1}+R_{C2}+4Rs+R_L\right);$ $P_{c6}=\frac{4(\frac{T}{2}-2t_6)}{T}p_{c6}$

i_0, i_{C1}, and $i_{C2} = i_{C3}$ are derived as specified in the third column of the table. These current values are then utilized to determine the power dissipation across each resistive component in the circuit.

$$p_{Con_+1} = i_o^2 R_{eq_+1_io} + i_{C1}^2 R_{eq_+1_ic1} + i_{C2}^2 R_{eq_+1_ic2} \tag{8}$$

The total resistance encountered along the conduction path of each loop in the equivalent circuit is characterized as the corresponding equivalent resistance and is defined for each case as follows:

$$\begin{aligned} R_{eq_+1_io} &= R_{C3} + 2R_S + R_L \\ R_{eq_+1_c1} &= R_{C1} + R_D + R_S \\ R_{eq_+1_c2} &= R_{C2} + R_{C3} + 2R_D + R_S \end{aligned} \tag{9}$$

In the waveform shown in Fig. 3, the +1 level appears once in the rising and once in the falling segment of the positive half-wave, and both time intervals are equal. Therefore, the total duration of the +1 level is given by $\sum \Delta t_{+1} = 2(t_2 - t_1)$. Based on (6), the corresponding average power is calculated as:

$$P_{Con_+1} = \frac{2(t_2 - t_1)}{T} p_{Con_+1} \tag{10}$$

The real-time and mean conduction losses for all remaining output levels are detailed in Column 4 of Table 2. The aggregate conduction loss is subsequently computed through (4) using the tabulated parameters. Due to identical circuit topologies at the ±2, ±4, and ±6 voltage levels, their respective power loss calculations are consolidated.

B. CALCULATION OF SWITCHING LOSSES, P_{SW}

As illustrated in Fig. 4, although the switching pulse appears to exhibit abrupt transitions, both turn-on and turn-off events occur over finite time intervals, denoted as ton and toff. These transitions involve dynamic changes in switch voltage and current, as shown in Fig. 5. During these periods, overlapping voltage and current result in energy dissipation, represented by the shaded areas in the figure. These switching events contribute to the total switching loss, defined as $P_{SW} = P_{on} + P_{off}$.

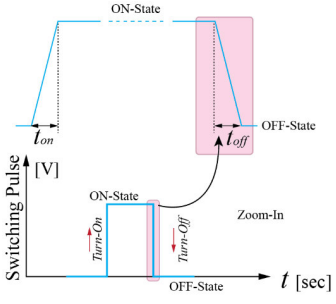


FIGURE 4. Illustration of the fundamental structure and timing of a switching pulse.

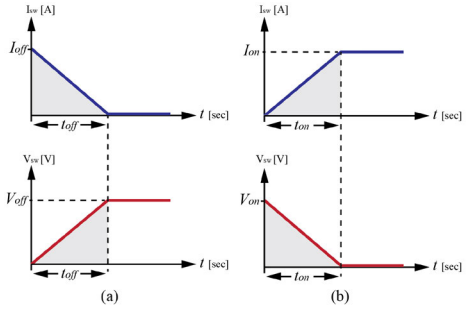


FIGURE 5. Voltage and current transition profiles of the switching device.

Turn-on loss: Initially, when the switch is in the OFF state, it sustains the full voltage Von with zero current. During the transition to the ON state, the voltage across the switch linearly drops to zero while the current linearly rises to IonI_{on}Ion, as depicted in Fig. 5(b). Assuming linear transitions for both voltage and current, the energy loss for the *i-th* switch can be calculated using the expression provided in [12].

$$\begin{aligned} E_{i,on} &= \int_0^{t_{on}} v(t) i(t) dt \\ &= \int_0^{t_{on}} V_{SWon,i}\left(\frac{t_{on} - t}{t_{on}}\right) I_{SWon,i}\left(\frac{t}{t_{on}}\right) dt \\ &= \frac{1}{6} V_{SWon,i} I_{SWon,i} t_{on} \end{aligned} \tag{11}$$

Here, $I_{SWon,i}$ denotes the current through the *i*-th power switch, and $V_{SWon,i}$ represents the switch voltage during the turn-on process. The parameter t_{on} refers to the duration of the turn-on interval.

Turn-off loss: During the transition from the ON to the OFF state, the switch current I_{off} decreases to zero, while the voltage across the switch rises from zero to V_{off}. This dynamic behavior, illustrated in Fig. 5(a), results in energy dissipation. Assuming linear variations in voltage and current, the turn-off energy loss for the *i-th* power switch during the toff interval can be calculated as follows.

$$\begin{aligned} E_{i,off} &= \int_0^{t_{off}} v(t) i(t) dt \\ &= \int_0^{t_{off}} V_{SWoff,i}\left(\frac{t_{off} - t}{t_{off}}\right) I_{SWoff,i}\left(\frac{t}{t_{off}}\right) dt \\ &= \frac{1}{6} V_{SWoff,i} I_{SWoff,i} t_{off} \end{aligned} \tag{12}$$

where $I_{SWoff,i}$ and $V_{SWoff,i}$ denote the current through and the voltage across the *i*-th switch during the turn-off interval, respectively, and toff represents the duration of the turn-off transition.

The total switching loss over one period is obtained by summing the losses of all individual switches, as expressed in (13). Let $N_{on,i}$ and $N_{off,i}$ represent the number of turn-on and turn-off events for the *i*-th switch within a period. Accordingly, the total energy dissipated by the *i*-th switch

during these transitions is given by (14).

$$E_{i,SW} = \sum_{T} (E_{i,on} + E_{i,off}) \tag{13}$$

$$E_{i,SW} = N_{on,i}E_{i,on} + N_{off,i}E_{i,off} \tag{14}$$

Equations (15) and (16) are used to determine the mean switching power loss and the cumulative switching power associated with each individual switch over a period.

$$P_{i,SW} = \frac{1}{T}E_{i,SW} \tag{15}$$

$$P_{SW} = \sum_{j=1}^{10} P_{j,SW} \tag{16}$$

C. CAPACITOR RIPPLE LOSS, P_R

In SC-MLI circuits, capacitor voltage ripples introduces additional power losses, referred to as ripple losses (P_{Ripple}). Estimating this loss requires first determining the ripple voltage.

$$\Delta v_C = \frac{1}{C}\int_{MDT} i_{C_{discharge}}(t)dt \tag{17}$$

Here, the ripple voltage depends on the capacitor's discharge current and the maximum discharging duration (MDT). The ripple power loss associated with each capacitor can be evaluated using:

$$P_{R,i} = \frac{1}{2}f_o \sum_{i}^{N_c} (C_i \Delta v_{C_i}^2) \tag{18}$$

$$P_R = \sum_{j=1}^{3} P_{R,j} \tag{19}$$

Based on this analysis, the overall loss and efficiency of the topology can be analytically modeled using the theoretical framework presented in (3) and (20).

$$\eta = \frac{P_{out}}{P_{out} + P_{Loss}} \tag{20}$$

Accurate loss estimation is essential for assessing inverter performance across different load scenarios. Unlike conventional approaches using simplified linear approximations, this study implements component thermal modeling to achieve more precise power loss characterization in power electronic systems. The loss analysis was performed using PLECS simulation software, which offers advanced thermal modeling capabilities for semiconductor devices to ensure high-fidelity loss calculations. Key parameters for the efficiency evaluation include: $C_1 = 2200\mu F$, $C_2 = C_3 = 1200\mu F$, $V_{DC} = 60V$. The resulting efficiency characteristics of the 13-level switched-capacitor multilevel inverter are presented in Fig. 6, demonstrating its performance across various output power levels.

The inverter was experimentally evaluated under resistive load conditions ranging from 100W to 1000W, and a peak efficiency of 97.10% was recorded within this operating range. Furthermore, it is observed that efficiency tends to decrease as the output power increases, indicating the impact of rising conduction and switching losses under heavier load conditions.

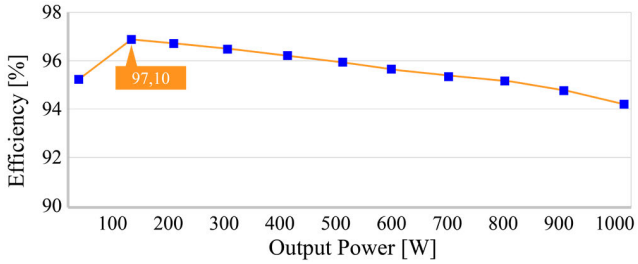


FIGURE 6. Variation of inverter efficiency with respect to output power.

Fig. 7 presents the power loss allocation across different components in the proposed multilevel inverter configuration. The analysis reveals that capacitors, diodes, and switching elements S_1' and S_3 account for the predominant portion of energy losses. As indicated in Table 1, these components remain active during capacitor charging operations, with switches S_1' and S_3 along with diodes D_1, D_2, and D_3 forming the conduction path. The substantial power dissipation in these components stems primarily from capacitor voltage ripple effects during charging cycles.

The fundamental frequency operation of the SC-MLI, implemented through NLC modulation, results in minimal switching losses. Fig. 8 demonstrates the relationship between output voltage levels and the corresponding voltage stress on power semiconductor devices.

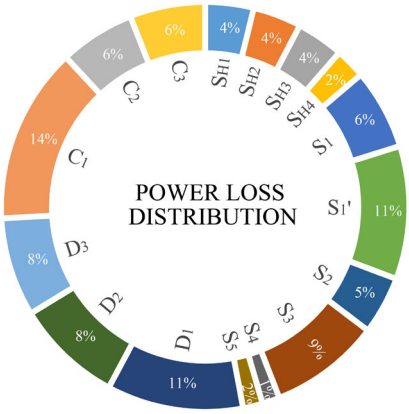


FIGURE 7. Power loss distribution among the power devices.

IV. COMPARATIVE STUDY

A thorough performance and cost analysis has been conducted for the proposed SC-MLI topology, comparing it with recent advanced multilevel inverter designs. In the cost function formulation, component efficiency is inherently considered through its influence on total power loss, thermal requirements, and system-level performance. Hence, the use

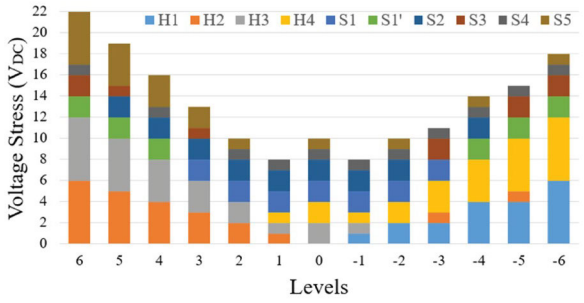


FIGURE 8. Voltage stress experienced by power switches in the proposed multilevel inverter.

of high-efficiency components contributes to a lower overall cost function value. The evaluation criteria, presented in Table 3, focus on essential design parameters including the number of DC sources (N_{DC}), power switches (N_{SW}), diodes (N_D), and capacitors (N_C). The study also examines critical electrical stress factors such as the peak inverse voltage (PIV) and total standing voltage (TSV) across power components. This comprehensive comparison provides valuable insights into the relative merits of different multilevel inverter configurations. To assess the economic and structural feasibility, a CF is employed, which integrates multiple parameters with weighting coefficients commonly adopted in literature. While some studies prioritize components in charging current path, others consider the maximum number of simultaneously conducting switches as a factor influencing CF. The CF for each topology is calculated using (21):

$$CF = \frac{(N_{SW} + N_{GD} + N_D + N_C + \gamma PIV_{pu} + \alpha TSV_{pu})N_{DC}}{N_L} \tag{21}$$

In this formulation, the weighting coefficients are set as $\gamma = 0.5$, $\alpha = 0.5$ and alternatively as $\gamma = 1.5$, $\alpha = 1.5$, to evaluate different design priorities. The normalized values of PIVpu and TSVpu are determined for each topology according to (22) and (23):

$$PIV_{pu} = \frac{PIV}{V_{Peak,Out}} \tag{22}$$

$$TSV_{pu} = \frac{TSV}{V_{Peak,Out}} \tag{23}$$

The proposed topology achieves a voltage gain of 3 and generates 13 output levels using only a single DC source, while requiring just 11 power switches, 10 gate drivers, 3 diodes, and 3 capacitors. Among all reviewed topologies, this configuration demonstrates one of the TSVpu across both $\alpha = 0.5$ and $\alpha = 1.5$ scenarios, with values of 2.36 and 2.92, respectively. This indicates superior compactness and component efficiency.

Notably, CF, a weighted indicator reflecting complexity and implementation burden, is also among the lowest (2.36), reinforcing the practicality of the design. In terms of efficiency, the proposed topology achieves 97.2% at 150 W, which is highly competitive, especially given the reduced component count.

Compared to earlier works such as [12] and [23], which achieve the same number of output levels but require more than 14 switches, multiple DC sources, and up to 4 capacitors, the proposed topology stands out by significantly reducing hardware requirements while maintaining high voltage gain and efficiency.

Furthermore, designs like [10] and [25] show comparable performance in terms of voltage gain and efficiency but still

TABLE 3. Comparison of various SC-MLI topologies with proposed topology.

P	Year	A_V	N_{DC}	N_L	N_{SW}	N_{GD}	N_D	N_C	PIV_{pu}	TSV_{pu}	CF		η%
											α=0.5	α=1.5	
[9]	2022	6	1	13	15	15	-	3	0.33	5.00	2.74	3.15	97.3 @1kW
[10]	2022	3	1	13	13	13	3	3	0.33	2.33	2.56	2.77	98.0 @0.2kW
[12]	2021	3	2	13	14	14	2	4	1.00	5.67	5.74	6.77	91.0 @1kW
[17]	2022	6	1	13	14	14	4	3	0.50	5.50	2.92	3.38	96.7 @1kW
[23]	2019	6	2	13	16	16	-	4	1.00	5.67	6.05	7.08	92.1 @1kW
[24]	2020	3	1	13	19	18	-	4	1.00	6.67	3.45	4.04	96.8 @1kW
[25]	2023	2	1	13	13	13	-	3	0.33	2.83	2.35	2.60	98.1 @0.3kW
[26]	2022	3	1	13	14	13	-	3	0.33	2.75	2.43	2.66	95.05 @1kW
[27]	2021	6	1	13	13	13	2	3	0.50	5.16	2.60	3.04	97.5 @2kW
[28]	2021	6	1	13	13	13	2	3	0.50	5.33	2.61	3.06	97.3 @1kW
[29]	2021	3	1	13	12	12	4	4	0.33	4.67	2.65	3.04	95.3 @1kW
[30]	2022	2	2	13	12	10	-	2	0.50	4.00	4.04	4.73	94.5 @0.9kW
P	**2025**	**3**	**1**	**13**	**11**	**10**	**3**	**3**	**1.00**	**6.33**	**2.36**	**2.92**	**97.2 @0.15kW**

A_V: Voltage gain, N_L: Number of output level, N_{DC}: Number of input source, N_{SW}: Number of power switches, N_{GD}: Number of gate drivers, N_D: Number of diodes, N_C: Number of capacitors, CF: Cost function, η: Efficiency

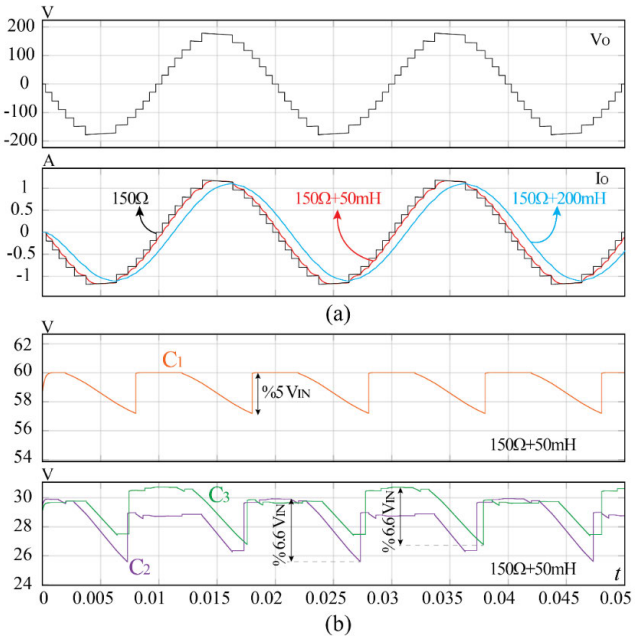


FIGURE 9. Performance of the proposed SC-MLI: (a) output voltage/ current under different loads; (b) capacitor ripple voltages.

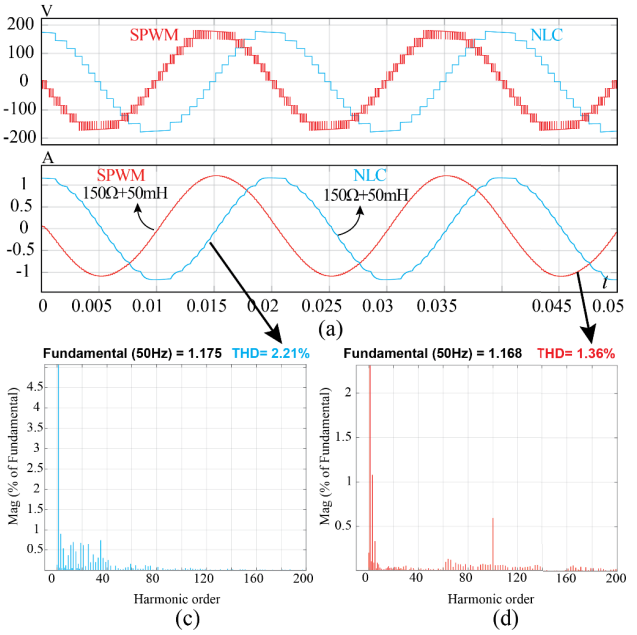


FIGURE 10. Analysis of the proposed SC-MLI under SPWM and NLC controls: (a) voltage and current response; (b) current THD evaluation.

use either equal or more switches and diodes. The proposed topology uniquely balances component minimization with performance, offering a viable and scalable solution for compact, single-source renewable and vehicular applications.

Additionally, compared to [30], which uses 12 switches and achieves lower voltage gain despite employing two DC sources, the proposed topology demonstrates superior efficiency and a more compact structure using only a single source. This further highlights the design's advantage in minimizing hardware while maintaining high performance and scalability.

V. SIMULATION AND EXPERIMENTAL VERIFICATION

A. SIMULATION RESULTS

Simulation models of the proposed SC-MLI topology were developed using both MATLAB/Simulink and PLECS environments to evaluate its performance under two distinct modulation strategies. Consistent circuit parameters were employed across both platforms to ensure result validity. The input DC voltage was set to 60V, and the capacitor values were determined through theoretical analysis, with $C1 = 2200\mu F$ and $C_2 = C_3 = 1200\mu F$. All capacitors were modeled with an equivalent series resistance (ESR) of 0.08 Ω.

The inverter was tested under various load conditions, switching frequencies, and modulation indexes (MI) using NLC and SPWM techniques. As depicted in Fig. 9(a), the inverter was simulated under three different load scenarios; resistive (150 Ω), RL (150 Ω + 50 mH), and heavily inductive (150 Ω + 200 mH); with the NLC method. The output voltage waveform successfully synthesizes 13 discrete levels, while the current waveform remains stable and continuous under all load conditions.

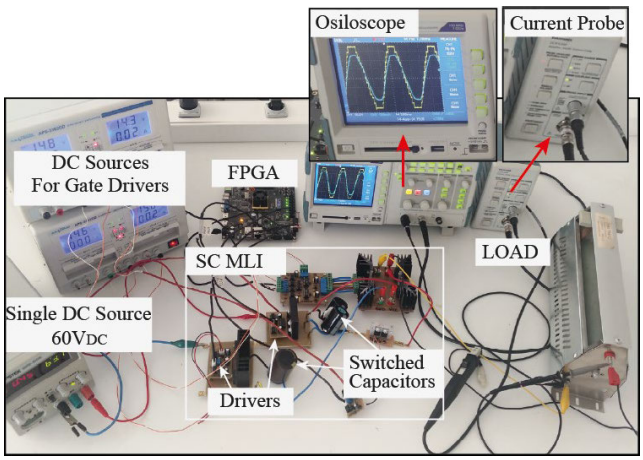


FIGURE 11. Laboratory prototype and test bench configuration for the 13-level SC-MLI.

Fig. 9 (b) presents the voltage ripple characteristics of the flying capacitors during operation. The ripple voltage for each capacitor remains within acceptable limits, staying below the 10% threshold, which validates the capacitor sizing and overall stability of the proposed configuration.

The proposed SC-MLI was evaluated under a low-inductive load of 150 Ω + 50 mH using both Sinusoidal Pulse Width Modulation (SPWM) and Nearest Level Control (NLC) techniques. To assess the quality of the output current waveform, a detailed harmonic analysis was conducted. As illustrated in Fig. 10(a), the output current waveform obtained under SPWM control closely resembles an ideal sinusoidal shape, demonstrating excellent waveform fidelity under the given load conditions. Similarly, the NLC-based

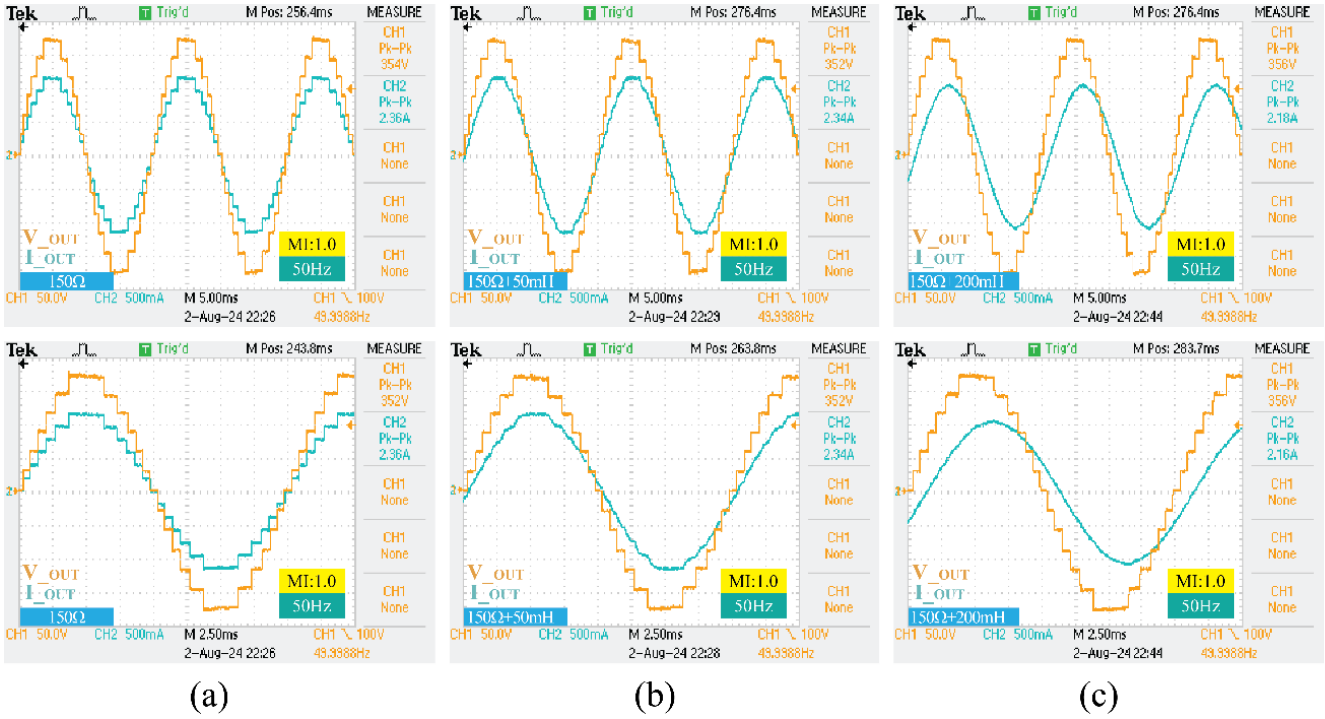


FIGURE 12. Pure resistive and resistive-inductive load test, (a) with 150Ω, (b) with 150Ω + 50 mH, (c) with 150Ω + 200 mH.

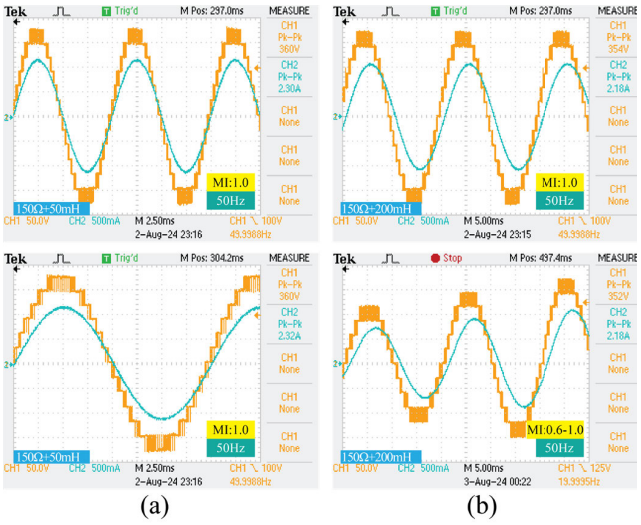


FIGURE 13. SPWM output waveforms, (a) with 150Ω + 50 mH, (b) with 150Ω + 200 mH.

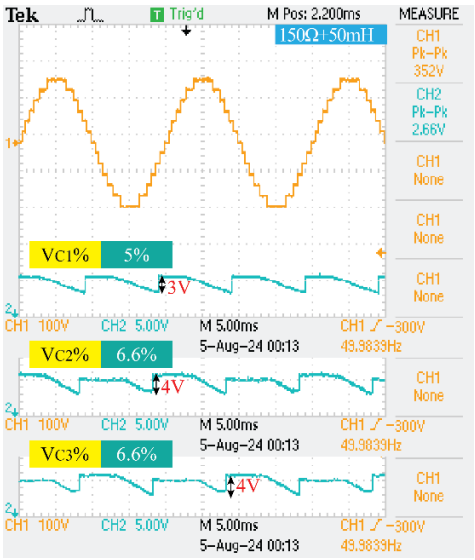


FIGURE 14. Voltage waveforms of the SCs and output voltage.

waveform also exhibits a satisfactory level of smoothness, indicating acceptable performance in practical scenarios.

The corresponding harmonic spectra presented in Fig. 10(b) reveal that the Total Harmonic Distortion (THD) of the output current is 1.36% for SPWM and 2.21% for NLC. Despite the slightly higher THD observed in the NLC case, the high-resolution multilevel output achieved through the proposed topology ensures that the waveform quality remains within acceptable limits. The results confirm that the inverter complies with relevant harmonic standards even without relying on high-frequency switching strategies, thereby validating the effectiveness and practical viability of the proposed SC-MLI architecture.

B. EXPERIMENTAL RESULTS

The hardware implementation of the 13-level SC-MLI is illustrated in Fig. 11, with detailed component specifications provided in Table 4. For switch control, the prototype employs a Genesys 2 Kintex-7 FPGA development

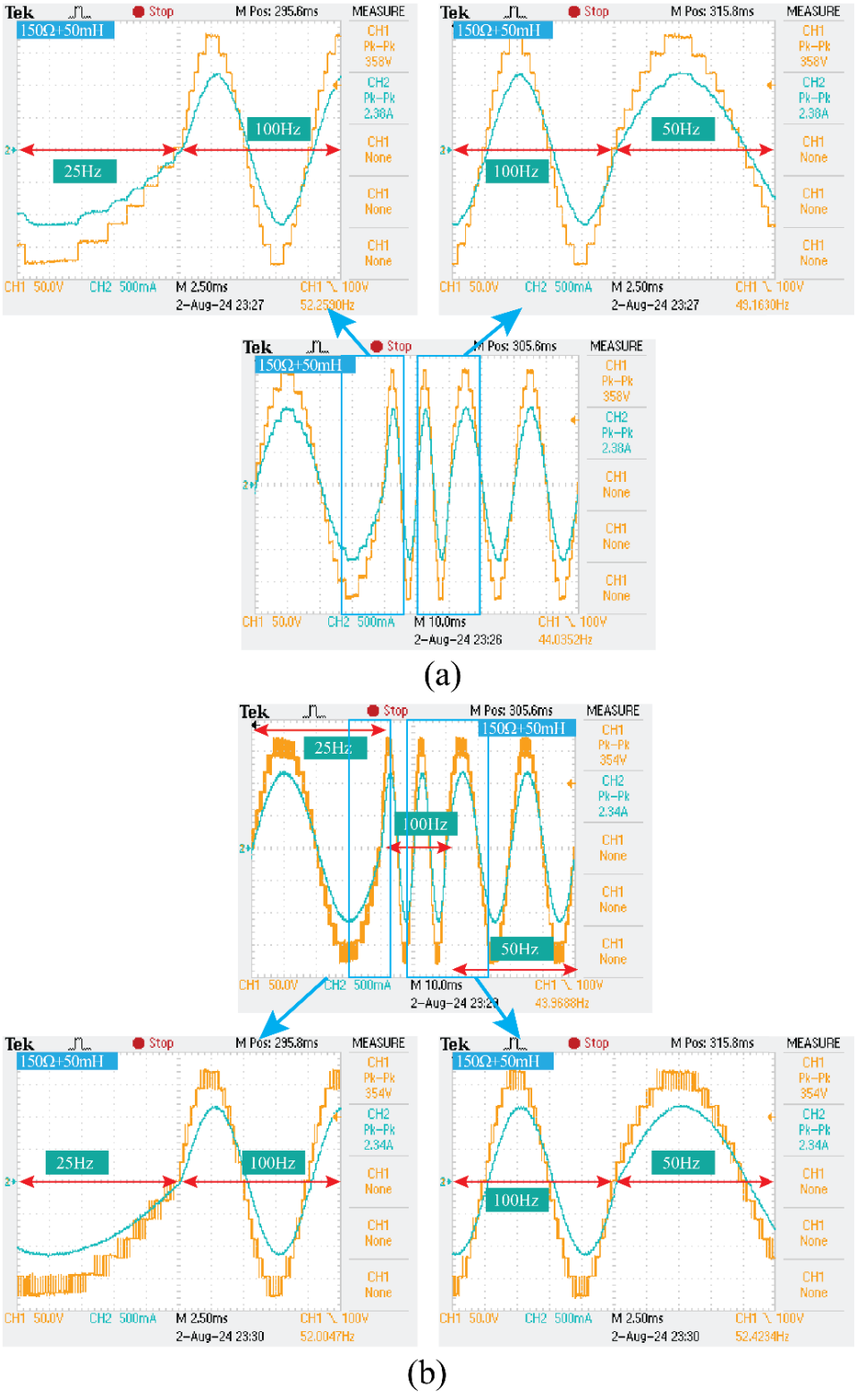


FIGURE 15. Dynamic response of the proposed 13-level SC-MLI to fundamental frequency variations: output voltage and current waveforms under different frequency transitions.

board to generate gate drive signals, ensuring accurate and flexible switching operation through programmable logic. The prototype was evaluated under both purely resistive and resistive-inductive load conditions. Furthermore, the inverter's output voltage waveform was observed to maintain consistent multilevel structure across varying MIs and



FIGURE 16. Response of the proposed 13-level MLI output current and voltage waves to MI and frequency changes.

TABLE 4. Parameters and component specifications.

PARAMETERS	
Input Voltage, Vdc	60V
Output Voltage	180V (peak)
Frequency	50 Hz
Max. Output Power	1000W
COMPONENTS	
C1	PG6DI (2200 µF, 600V, ESR=80 mΩ)
C2-C3	PG6DI (1200 µF, 600V, ESR=80 mΩ)
L1-L2-C3	80 µH
IGBT	IGW60N60H3 (VCE=600 V, IC=60A)
Fast Recovery Diode	DSEI 60-06 (IFAV=60A, VRRM=600V)
Controller	FPGA Dev. Board (Genesys 2 Kintex-7)
Output Loads	Resist. (150Ω), Ind. (50mH+200mH)

switching frequencies. The experimental results closely align with the simulation outcomes, thereby validating the operational accuracy and robustness of the proposed topology.

The NLC control signals are generated at a frequency of 50Hz and full MI using the FPGA-based control platform. The experimental prototype was initially tested under a purely resistive load of 150 Ω. The corresponding voltage and current waveforms are illustrated in Fig. 12(a). To evaluate the inverter's dynamic performance under inductive loading, additional tests were performed by connecting inductors of 50 mH and 200 mH in series with the resistive load. The impact of increasing load inductance on the output waveforms is demonstrated in Fig. 12(b) and Fig. 12(c), respectively, highlighting the system's capability to maintain waveform quality under varying load conditions.

The output waveforms of the experimental test using inductive loads and the SPWM technique are presented in Fig. 13. One of the important issues in SC circuits is the fluctuation in capacitor voltages. According to the capacitance values determined according to theoretical calculations, the experimental prototype is realized with the NLC method and 150 Ω + 50 mH load. The voltages on the capacitors V_{C1}, V_{C2} and V_{C3} are shown in Fig. 14.

To evaluate the dynamic response of the proposed SC-MLI under varying frequency conditions, Fig. 15 illustrates the inverter's performance when subjected to fundamental frequency shifts. The experimental prototype was tested using both NLC and SPWM control methods while maintaining a constant RL load. In Fig. 15(a) and 15(b), the output voltage and current waveforms are shown for frequency transitions from 25Hz to 100Hz and from 100Hz back to 25Hz, respectively. The results demonstrate that the proposed inverter retains waveform integrity throughout the frequency changes.

Fig. 16 presents the effect of MI variation on inverter performance. The 13-level SC-MLI is operated with sequential MI values of 0.3, 0.6, and 1.0, before returning to 0.3. The output waveform remains stable and consistent throughout

the MI changes, indicating robust control behavior. As with the frequency tests, detailed views of the transition regions are provided to observe transient behavior more closely.

VI. CONCLUSION

This paper introduces a novel single-source SC-MLI topology capable of generating 13 output voltage levels with a voltage gain of three. The proposed 13-level SC-MLI is rigorously compared with recent state-of-the-art topologies from the past six years, evaluating key performance metrics including the number of DC sources, switched capacitors, power switches, diodes, total standing voltage, peak inverse voltage, and cost function. Compared to existing single-source configurations, the proposed design achieves significant reductions in component count - particularly in capacitors, switches, and diodes - resulting in notable advantages in terms of system complexity, cost-effectiveness, and practical implementation. Furthermore, the topology features inherent self-voltage balancing capability for the capacitors, eliminating the need for additional voltage sensors or dedicated balancing circuits. These combined improvements make the proposed SC-MLI a competitive solution for medium-voltage power conversion applications. The proposed inverter is evaluated under both NLC and SPWM modulation schemes. Theoretical analysis, simulation results, and experimental findings demonstrate high consistency, validating the feasibility and reliability of the design. Loss and efficiency assessments are conducted using PLECS with detailed thermal models, showing a peak efficiency of 97.2% in the 100–1000W power range. Experimental measurements yield a practical efficiency of 95.3%. Overall, the findings confirm that the proposed 13-level SC-MLI satisfies harmonic standards, achieves high efficiency, and maintains a low component count, making it a highly competitive and practical solution for advanced multilevel inverter applications. Finaly, future work will address closed-loop control and grid-connected applications to explore its potential in medium- and high-power systems.

DECLARATION OF CONFLICT OF INTEREST

The authors declare that they have no conflict of interest that could have appeared to influence the work reported in this article.

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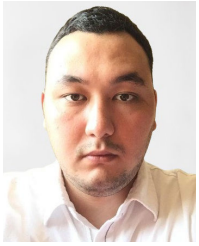
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